6-Channel Buffer with High Power V_{COM}

The EL5624A integrates six gamma reference buffers with a single high power V_{COM} amplifier. Each gamma buffer has a bandwidth of 12MHz and features a slew rate of 15V/µs. The output current is rated at 30mA continuous, 140mA peak.

The V_{COM} amplifier is rated for 260mA peak output current and also features higher slew rate (70V/µs) and bandwidth (35MHz) for use in error cancellation circuits.

The EL5624A is available in the 20-pin HTSSOP package and is specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (See Note)	PACKAGE (Pb-Free)	TAPE & REEL	PKG. DWG. #
EL5624AIREZ (See Note)	20-Pin HTSSOP (Pb-free)	-	MDP0048
EL5624AIREZ-T7 (See Note)	20-Pin HTSSOP (Pb-free)	7"	MDP0048
EL5624AIREZ-T13 (See Note)	20-Pin HTSSOP (Pb-free)	13"	MDP0048

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

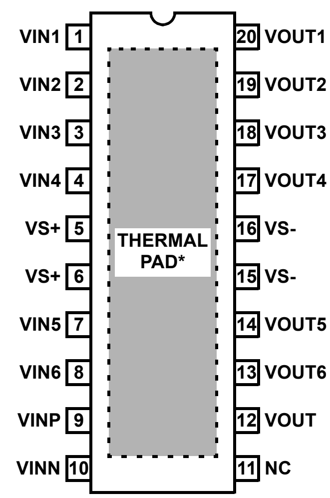
- 6 x gamma buffers
- Single high power V_{COM} amplifier
- 260mA peak V_{COM} output current
- Low power - just 8.5mA
- Pb-free available (RoHS compliant)

Applications

- TFT-LCD displays
- Flat panel monitors
- Notebook displays
- LCD-TVs

Pinout

EL5624A
(20-PIN HTSSOP)
TOP VIEW



*** THERMAL PAD CONNECTED TO PIN 15 or 16 (V_S-)**

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . . +18V
Input Voltage . . . . V_S- -0.5V, V_S+ +0.5V
Maximum Continuous Output Current (Buffer) 30mA
Maximum Continuous Output Current (V_{COM}) 60mA

Power Dissipation . . . . See Curves
Maximum Die Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C
Operating Conditions . . . . -40°C to +85°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +15V, V_S- = 0, R_L = 10kΩ, C_L = 10pF to 0V, Gain of V_{COM} = 1, RLV_{CM} = 1kΩ and T_A = 25°C, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	14	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	1V ≤ V_{OUT} ≤ 14V	0.992		1.008	V/V
INPUT CHARACTERISTICS (V_{COM} AMPLIFIER)						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		1	15	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
V_{REG}	Load Regulation	V_{COM} = 1.5V, -60mA < I_L < 60mA	-20		+20	mV
A_{VOL}	Open Loop Gain	R_L = 1kΩ	55	75		dB
CMRR	Common Rejection Ratio		45	70		dB
OUTPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OL}	Output Swing Low	I_L = 7.5mA		50	150	mV
V_{OH}	Output Swing High	I_L = 7.5mA	14.85	14.95		V
I_{SC}	Short Circuit Current	R_L = 10Ω	±200	±250		mA
OUTPUT CHARACTERISTICS (V_{COM} AMPLIFIER)						
V_{OL}	Output Swing Low	I_L = -7.5mA		50	150	mV
V_{OH}	Output Swing High	I_L = +7.5mA	14.85	14.95		V
I_{SC}	Short Circuit Current	R_L = 10Ω	±220	±260		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	Reference buffer V_S from 4.5V to 15.5V	55	80		dB
		V_{COM} buffer, V_S from 4.5V to 15.5V	55	80		dB
I_S	Total Supply Current	No load		8.5	10	mA
DYNAMIC PERFORMANCE (BUFFER AMPLIFIERS)						
SR	Slew Rate (Note 2)	-4V ≤ V_{OUT} ≤ 4V, 20% to 80%	50	70		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		250		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz

Electrical Specifications $V_S+ = +15V$, $V_S- = 0$, $R_L = 10k\Omega$, $C_L = 10pF$ to 0V, Gain of $V_{COM} = 1$, $RLV_{CM} = 1k\Omega$ and $T_A = 25°C$, unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GBWP	Gain-Bandwidth Product	$R_L = 10k\Omega$, $C_L = 10pF$		8		MHz
PM	Phase Margin	$R_L = 10k\Omega$, $C_L = 10pF$		50		°
CS	Channel Separation	f = 5MHz		75		dB
DYNAMIC PERFORMANCE (V_{COM} AMPLIFIERS)						
SR	Slew Rate (Note 2)	$-4V \leq V_{OUT} \leq 4V$, 20% to 80%	60	70		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 6V$ step		150		ns
BW	-3dB Bandwidth	$R_L = 1k\Omega$, $C_L = 2pF$		35		MHz
GBWP	Gain-Bandwidth Product	$R_L = 1k\Omega$, $C_L = 2pF$		20		MHz
PM	Phase Margin	$R_L = 1k\Omega$, $C_L = 2pF$		50		°

NOTES:

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	VIN1	Input
2	VIN2	Input
3	VIN3	Input
4	VIN4	Input
5, 6	VS+	Positive supply
9	VINP	Positive input - V_{COM}
10	VINN	Negative input - V_{COM}
11	NC	Not connected
12	VOUT	Output for V_{COM}
15, 16	VS-	Negative supply
17	VOUT4	Output
18	VOUT3	Output
19	VOUT2	Output
20	VOUT1	Output
7	VIN5	Input
8	VIN6	Input
14	VOUT5	Output
13	VOUT6	Output

Test Circuits

Typical Performance Curves

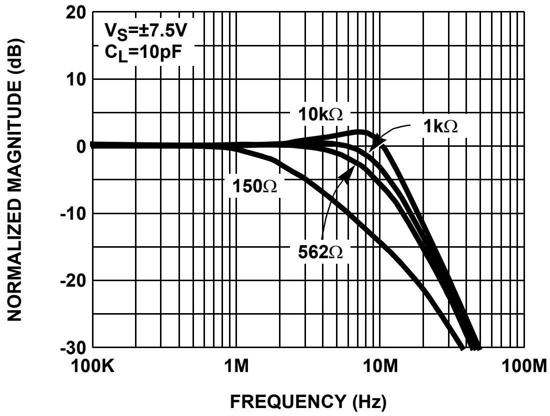


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS R_L (BUFFER)

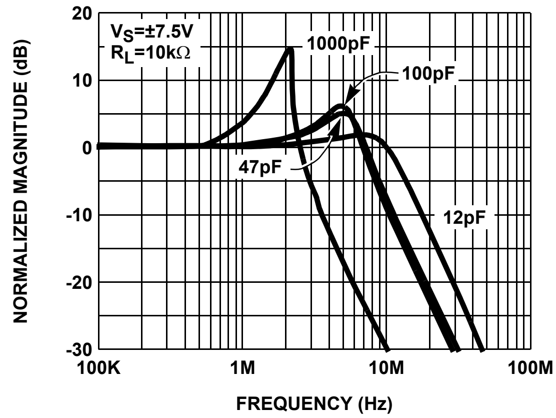


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS C_L (BUFFER)

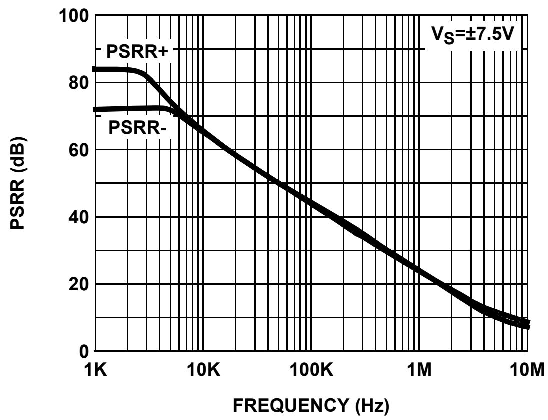


FIGURE 3. PSRR vs FREQUENCY (BUFFER)

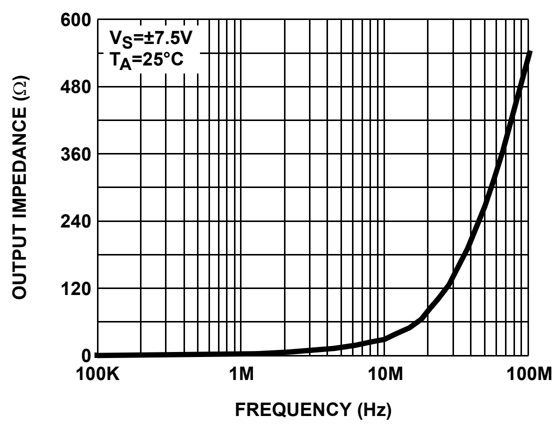


FIGURE 4. OUTPUT IMPEDANCE vs FREQUENCY (BUFFER)

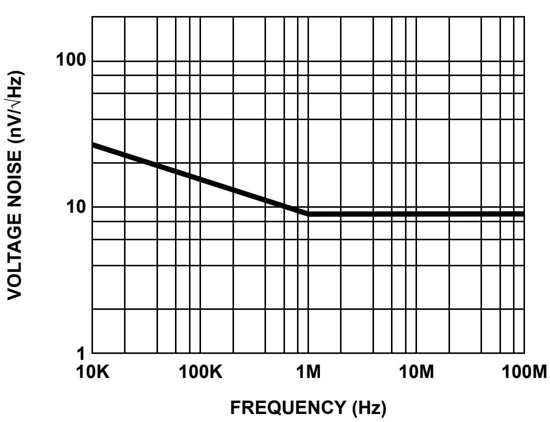


FIGURE 5. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (BUFFER)

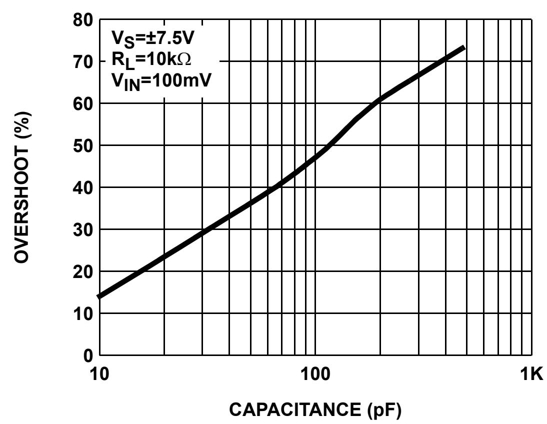


FIGURE 6. OVERSHOOT vs LOAD CAPACITANCE (BUFFER)

Typical Performance Curves (Continued)

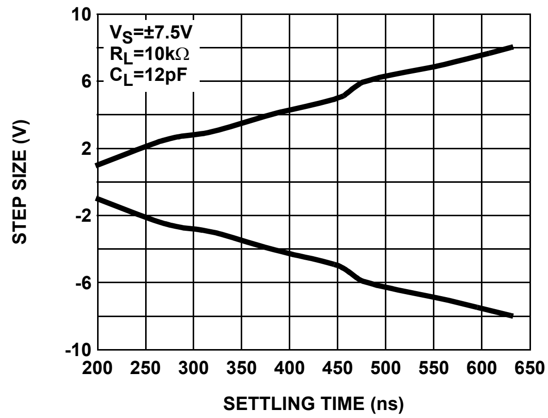


FIGURE 7. SETTLING TIME vs STEP SIZE (BUFFER)

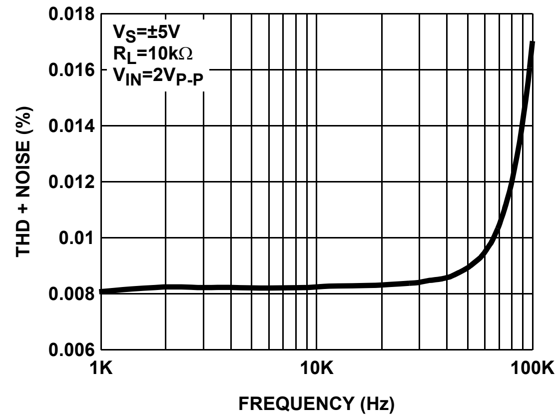


FIGURE 8. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (BUFFER)

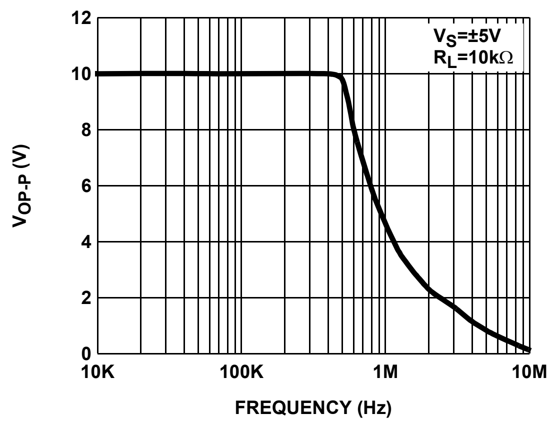


FIGURE 9. OUTPUT SWING vs FREQUENCY (BUFFER)

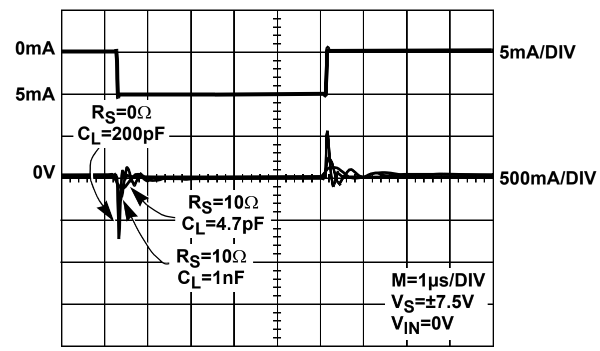


FIGURE 10. TRANSIENT LOAD REGULATION - SOURCING (BUFFER)

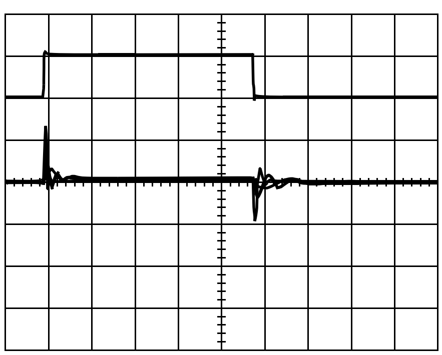


FIGURE 11. TRANSIENT LOAD REGULATION -SINKING (BUFFER)

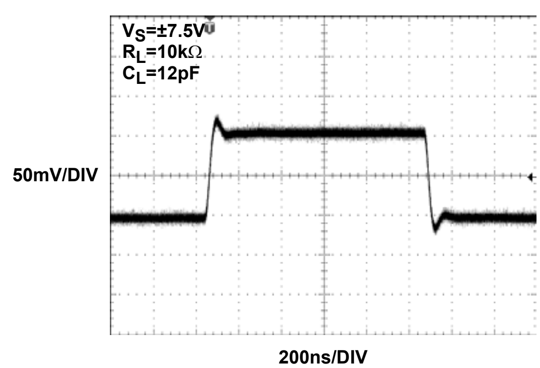


FIGURE 12. SMALL SIGNAL TRANSIENT RESPONSE (BUFFER)

Typical Performance Curves (Continued)

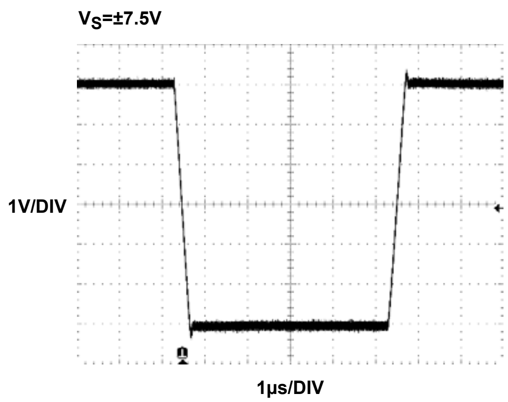


FIGURE 13. LARGE SIGNAL TRANSIENT RESPONSE (BUFFER)

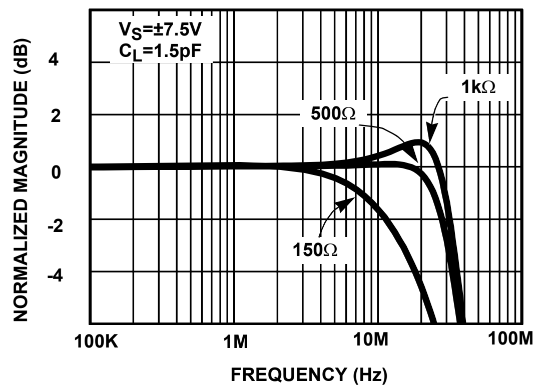


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS R_L (V_{COM})

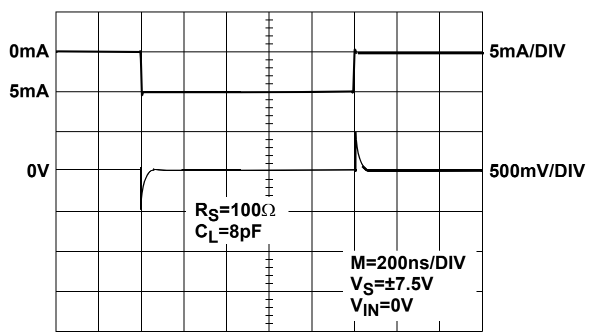


FIGURE 15. TRANSIENT LOAD REGULATION - SOURCING (V_{COM})

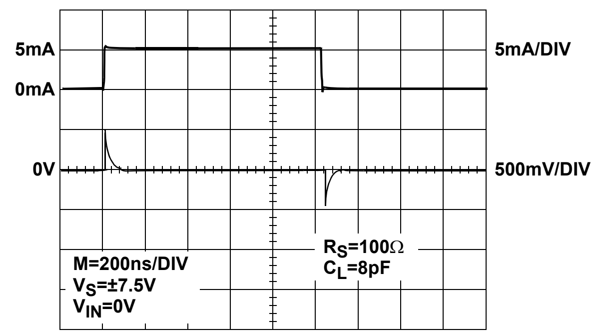


FIGURE 16. TRANSIENT LOAD REGULATION - SINKING (V_{COM})

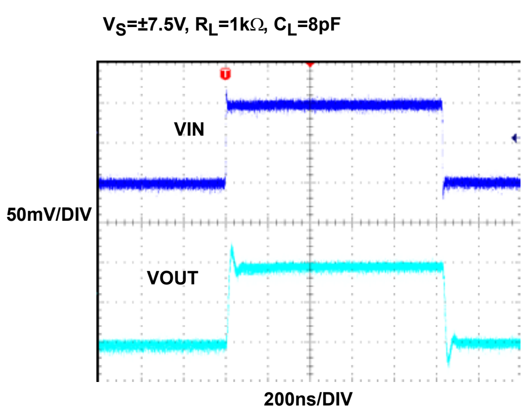


FIGURE 17. SMALL SIGNAL TRANSIENT RESPONSE (VCOM)

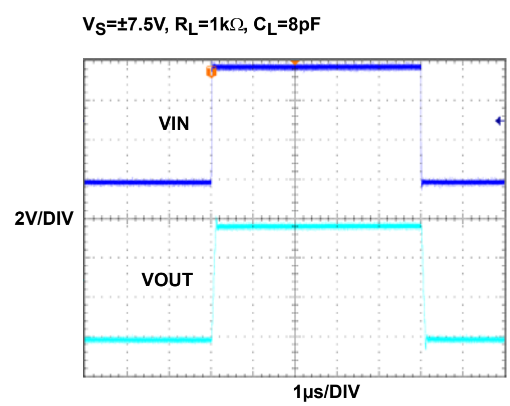


FIGURE 18. LARGE SIGNAL TRANSIENT RESPONSE (V_{COM})

Typical Performance Curves (Continued)

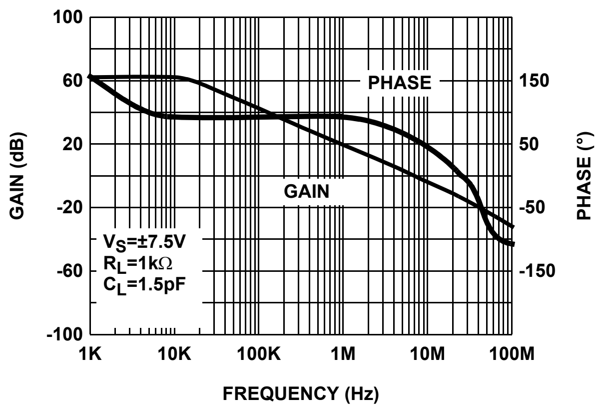


FIGURE 19. OPEN LOOP GAIN AND PHASE vs FREQUENCY

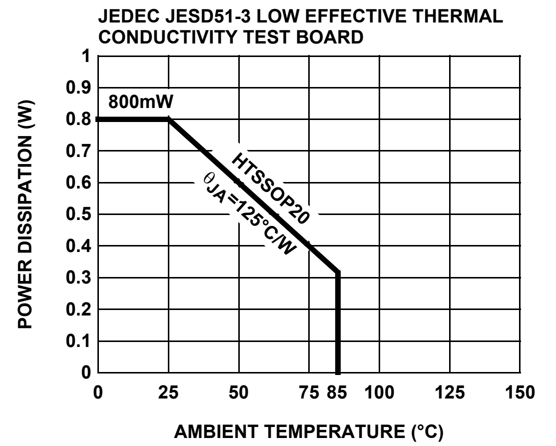


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

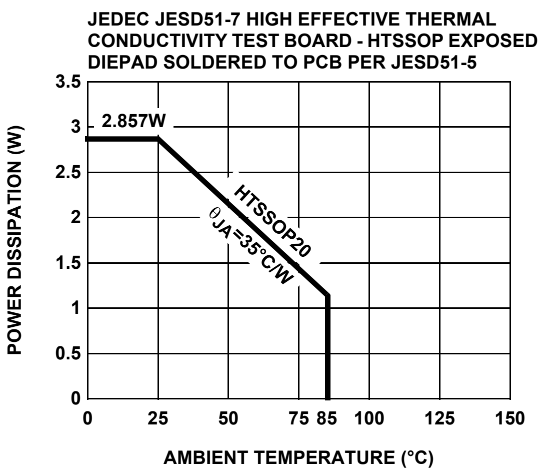


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Description of Operation and Application Information

Product Description

The EL5624A is fabricated using a high voltage CMOS process. It exhibits rail to rail input and output capability and has very low power consumption. When driving a load of 10K and 12pF, this buffer has a -3dB bandwidth of 12MHz and exhibit 18V/µs slew rate. The V_{COM} amplifier has a -3dB bandwidth of 35MHz and exhibit 70V/µs slew rate.

Input, Output, and Supply Voltage Range

The EL5624A is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range from 4.5V to 16.5V.

The input common-mode voltage range of the EL5624A extends 500mV beyond the supply rails. The output swings of the buffers and V_{COM} amplifier typically extend to within 100mV of the positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage even closer to each supply rails.

Output Phase Reversal

The EL5624A is immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diode placed in the input stage of the device begin to conduct and overvoltage damage could occur.

Choice of Feedback Resistor and Gain Bandwidth Product for V_{COM} Amplifier

For applications that require a gain of +1, no feedback resistor is required. Just short the output pin to the inverting input pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, the output stage is also a gain stage with the load. R_F and R_G appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum performance. For gain of +1, R_F = 0 is optimum. For the gains other than +1, optimum response is obtained with R_F between 1kΩ to 5kΩ.

The V_{COM} amplifier has a gain bandwidth product of 20MHz. For gains ≥5, its bandwidth can be predicted by the following equation:

$$Gain \times BW = 20MHz$$

Output Drive Capability

The EL5624A does not have internal short-circuit protection circuitry. The buffer will limit the short circuit current to over 250mA and the V_{COM} amplifier will limit the short circuit current to ±200mA if the outputs are directly shorted to the positive or the negative supply. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output continuous current never exceeds ±30mA for the buffers and ±60mA for the V_{COM} amplifier. These limits are set by the design of the internal metal interconnections.

The Unused Buffers

It is recommended that any unused buffers should have their inputs tied to ground plane.

Power Dissipation

With the high-output drive capability of the EL5624A, it is possible to exceed the 125°C “absolute-maximum junction temperature” under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_S + - V_{OUT}i) \times I_{LOAD}i] + (V_S + - V_{OUT}) \times I_{LA}$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_{OUT}i - V_S -) \times I_{LOAD}i] + (V_{OUT} - V_S -) \times I_{LA}$$

when sinking.

where:

- i = 1 to total number of buffers
- V_S = Total supply voltage of buffer and V_{COM}
- I_{SMAX} = Total quiescent current
- $V_{OUT}i$ = Maximum output voltage of the application
- V_{OUT} = Maximum output voltage of V_{COM}
- $I_{LOAD}i$ = Load current of buffer
- I_{LA} = Load current of V_{COM}

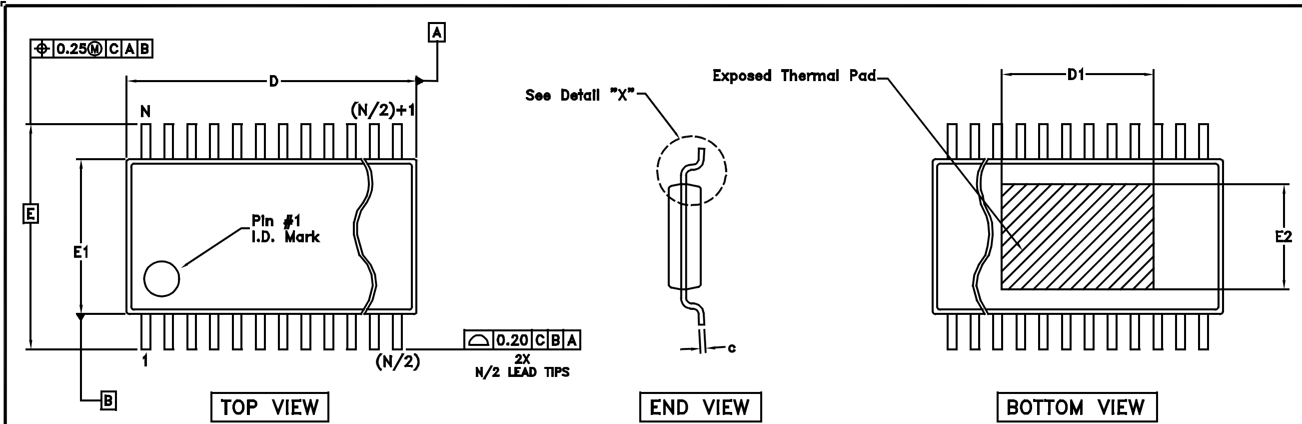
If we set the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

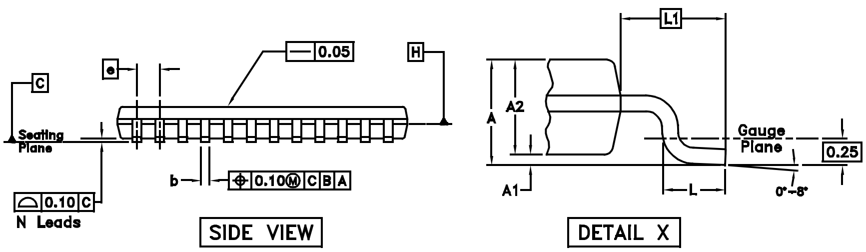
Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, one 0.1µF ceramic capacitor should be placed from the V_S+ pin to ground. A 4.7µF tantalum capacitor should then be connected from the V_S+ pin to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Important Note: The metal plane used for heat sinking of the device is electrically connected to the negative supply potential (V_S-). If V_S- is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad must be isolated from any other power planes.

Package Outline Drawing





DIMENSION TABLE					
Symbol	14L	20L	24L	28L	Tolerance
A	1.20	1.20	1.20	1.20	MAX.
A1	0.075	0.075	0.075	0.075	+/- 0.075
A2	0.90	0.90	0.90	0.90	+0.15/-0.10
D	5.00	6.50	7.80	9.70	+/- 0.10
E	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	+/- 0.10
L	0.60	0.60	0.60	0.60	+/- 0.15
L1	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	+0.05/-0.06
e	0.65	0.65	0.65	0.65	Basic
D1	3.2	4.2	4.3	5.0	Reference
E2	3.0	3.0	3.0	3.0	Reference
N	14	20	24	28	Reference

Drawing #: MDP0048	PACKAGE OUTLINE DRAWING HTSSOP (Heat-Sink TSSOP) Family
Rev: 1	
Date: 7/21/03	
Units: mm	
JEDEC Reg: MO-153	

Notes:

(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.

(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.

(3) Dimensions "D" and "E1" are measured at datum plane H.

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawings shown here may not be the latest versions. For the latest revisions, please refer to the Intersil website at www.intersil.com/design/packages/elantec

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com